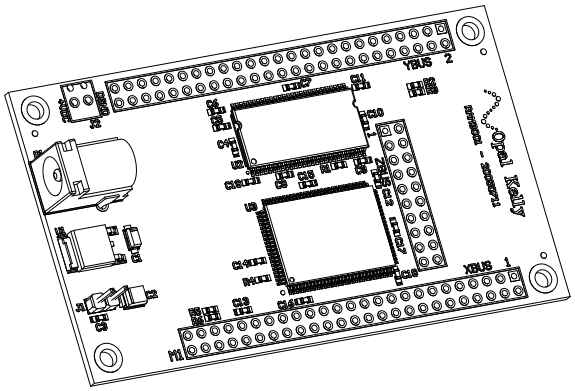
Opal Kelly



RAM3001 User's Manual

Versatile memory expansion for the XEM3001 with on-board voltage regulator for additional self-powered current.

The RAM3001 is a versatile memory expansion module for the XEM3001. Available in three assembly configurations, it is suitable for many FPGA applications requiring additional memory. The RAM3001-D is assembled with a 32 MB synchronous dynamic RAM (SDRAM). The RAM3001-S comes with a 512 kB synchronous static RAM (SSRAM). Finally, the RAM3001-DS is assembled with both memory devices. All three configurations come with a 1-A LDO regulator and DC power connector for applications which require more current than the USB bus current of 500 mA.

Software, documentation, samples, and related materials are

Opal Kelly Incorporated
3442 SE Ironwood Ave
Hillsboro, OR 97123
http://www.opalkelly.com

Revision History:

Date	Description
20050902	Initial release.
20070118	Fixed clock configuration typos.

Contents

Introducing the RAM3001

The RAM3001 is a versatile memory expansion module for the XEM3001. While the FPGA on-board the XEM3001 contains a considerable amount of available RAM, it is often not enough for certain applications.

The RAM3001 is availble in three different configurations, each suitable for different applications.

RAM3001-D: DRAM-only Configuration

The RAM3001-D contains a 32-MB (256-Mb) synchronous DRAM arranged in a 16-Meg x 16 configuration with 512-word pages. The DRAM has a CAS latency of 2 and maximum clock frequency of 143-MHz. Since it is a DRAM, it requires periodic refresh cycles to recharge the memory cells. Each of the 8192 rows must be refreshed every 64 ms to guarantee data integrity. To facilitate easier refresh logic design, the device includes autorefresh counters.

The DRAM is most efficiently accessed in burst transfers and provides programmable burst lengths of 1, 2, 4, or 8 locations as well as a full 512-word page (with optional short burst termination for shorter-than-512 bursts).

Timing and usage information for the DRAM device can be found in the Micron MT48LC16M16A2 datasheet or compatible device datasheets from other manufacturers.

In this configuration, only the XEM3001 YBUS (JP3) is used.

RAM3001-S: SRAM-only Configuration

The RAM3001-S contains a 256kx18 (4-Mb) synchronous SRAM. It is a NoBL (also called ZBT by other manufacturers) architecture which allows back-to-back read and write cycles. It has a maximum clock cycle of 133-MHz.

Timing and usage information for the SRAM device can be found in the Cypress CY7C1352G datasheet or compatible device datasheets from other manufacturers.

In this configuration, only the XEM3001 ZBUS (JP1) and XBUS (JP2) are used.

RAM3001-DS: DRAM and SRAM Configuration

The RAM3001-DS contains both SRAM and DRAM devices on the same board. In this configuration nearly all XEM3001 FPGA pins are consumed.

Power Supply

The XEM3001 may be configured in either bus-powered or self-powered mode. As a bus-powered device, it is recommended that the maximum USB bus current of 500 mA not be exceeded. Since the RAM3001 adds another device to the power supply, the RAM3001 also includes a power regulator and DC power jack that can provide up to 1 A to the RAM3001 and XEM3001.

IMPORTANT NOTE!!!! In order to use the RAM3001-supplied power, J1 on the RAM3001 must be inserted. In addition, J1 on the XEM3001 MUST BE REMOVED. If both jumpers are inserted, permanent damage may be done to either board and possibly the USB port on your PC.

Physical Arrangement

The RAM3001 was designed to be vertically stacked to the XEM3001. It can stack either below or above the XEM3001, depending on the user's preferred arrangement.

Clock Connections

Both the SDRAM and SRAM devices are synchronous devices and require a clock input from the XEM3001. There are several ways a designer may prefer to drive these clock signals. For example, the XEM3001 PLL may be configured to generate a clock which is routed at the board level to both the FPGA and RAM device. This is the default configuration of the RAM3001. Some designers may prefer to have the FPGA generate the clock signal and route it to the RAM device. Both configurations are supported by the RAM3001 design.

SRAM Clock

In the factory configuration, both R5 and R6 are inserted. This means that the PLL output SYS_CLK4 (XEM3001 JP3-48) drives the SRAM clock and also drives the FPGA's X_CLK1 input (FPGA pin P180). If you intend to use the FPGA to output a clock signal to the SRAM, you should remove R6.

Note that both R5 and R6 are removed in SDRAM-only configurations.

SDRAM Clock

In the factory configuration, both R2 and R3 are inserted. This means that the PLL output SYS_CLK5 (XEM3001 JP2-3) drives the SDRAM clock and also drives the FPGA's Y_CLK1 input (FPGA pin P184). If you intent to use the FPGA to output a clock signal to the SDRAM, you should remove R3.

Note that both R2 and R3 are removed for SRAM-only configurations.

SRAM Connections

The SSRAM is connected to the XEM3001 XBUS (JP3) and some pins of the XEM3001 ZBUS (JP1). Assuming both boards are stacked component-side up, the JP3 and JP1 pin numbers for the SSRAM connections are given in the tables below.

(*) CLK on the SSRAM is connected to SYS_CLK4, X_CLK1, and Z_BUS[0] through 0-Ohm resistors.

JP3 Pin	Signal	FPGA pin
1	DGND	
2	DGND	
3	D[2]	P156
4		
5	A[0]	P154
6		
7	A[1]	P150
8	A[2]	P149
9	+3.3VDD	
10	+3.3VDD	
11	A[3]	P148
12	A[4]	P147
13	A[5]	P146
14	MODE	P144
15	P[2]	P143
16	D[15]	P141
17	D[14]	P140

JP3 Pin	Signal	FPGA pin
18	D[13]	P139
19	DGND	
20	DGND	
21	D[12]	P138
22	D[11]	P137
23	D[10]	P135
24	D[9]	P133
25	D[3]	P132
26	D[8]	P131
27	D[4]	P130
28	ZZ	P128
29	D[6]	P126
30	D[5]	P125
31	DGND	
32	DGND	
33	P[1]	P124
34	D[7]	P123

JP3 Pin	Signal	FPGA pin
35	A[7]	P122
36	A[6]	P120
37	WEn	P119
38	CE1n	P117
39	OEn	P116
40	CENn	P115
41	+3.3VDD	
42	+3.3VDD	
43	A[8]	P114
44	ADV_LD	P113
45	A[10]	P111
46	A[9]	P109
47	CLK (*)	P180
48	CLK (*)	
49	DGND	
50	DGND	

JP1 Pin	Signal	FPGA pin
1	+3.3VDD	
2	+3.3VDD	
3	CLK (*)	
4	D[0]	P185
5	D[1]	P182
6	A[17]	P178
7	A[16]	P176
8	A[15]	P175
9	A[14]	P172
10	A[13]	P171

JP1 Pin	Signal	FPGA pin
11	A[12]	P169
12	A[11]	P168
13		
14		
15		
16		
17		
18		
19	DGND	
20	DGND	

SDRAM Connections

The SDRAM is connected exclusively to the XEM3001 YBUS (JP2). Assuming that the boards are stacked component-side up, the JP2 pin numbers for the SDRAM connections are given in the tables below.

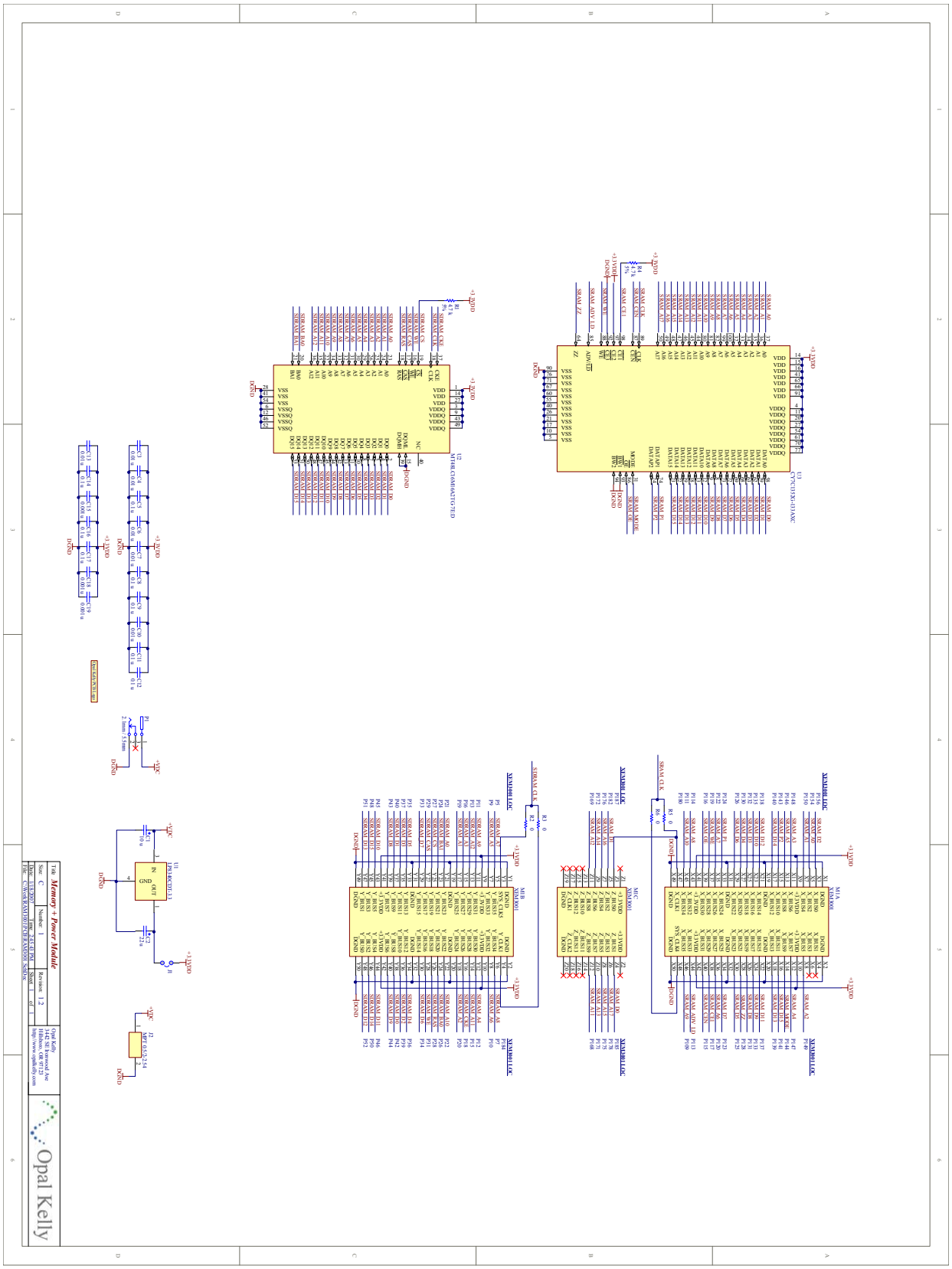
(*) CLK on the SDRAM is connected to both SYS_CLK5 and Y_CLK1 through 0-Ohm resistors.

JP2 Pin	Signal	FPGA Pin
1	DGND	
2	DGND	
3	CLK (*)	
4	CLK (*)	P184
5	A[7]	P5
6	A[8]	P7
7	A[5]	P9
8	A[6]	P10
9	+3.3VDD	
10	+3.3VDD	
11	A[9]	P11
12	A[4]	P12
13	A[12]	P13
14	A[11]	P15
15	A[3]	P16
16	CKE	P18
17	A[1]	P19

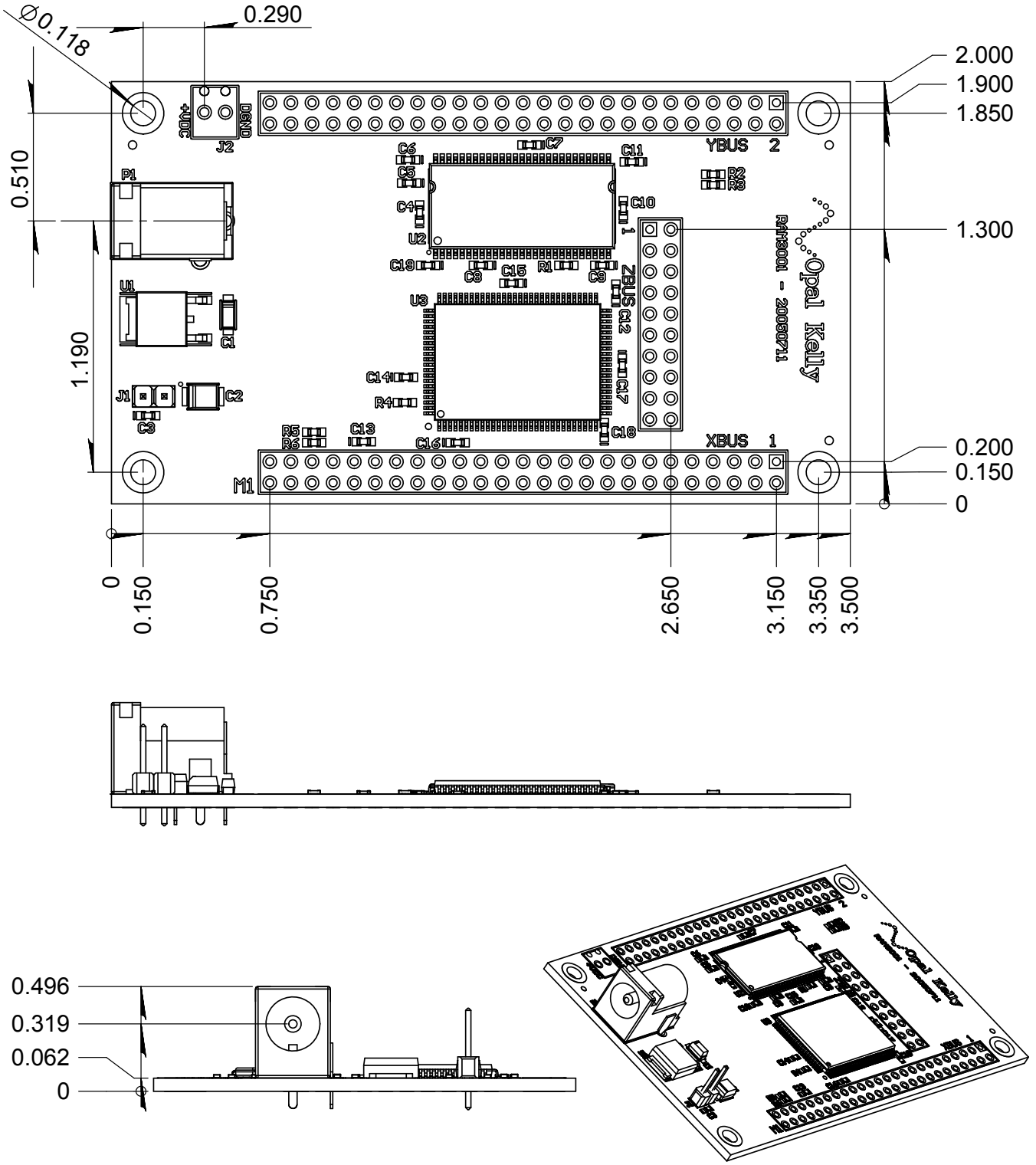
JP2 Pin	Signal	FPGA Pin
18	A[2]	P20
19	DGND	
20	DGND	
21	A[0]	P21
22	A[10]	P22
23	BA[1]	P24
24	BA[0]	P26
25	CSn	P27
26	RASn	P28
27	CASn	P29
28	WEn	P31
29	D[7]	P33
30	D[6]	P34
31	DGND	
32	DGND	
33	D[5]	P35
34	D[4]	P36

JP2 Pin	Signal	FPGA Pin
35	D[3]	P37
36	D[2]	P39
37	D[1]	P40
38	D[0]	P42
39	D[8]	P43
40	D[9]	P44
41	+3.3VDD	
42	+3.3VDD	
43	D[10]	P45
44	D[11]	P46
45	D[15]	P48
46	D[14]	P50
47	D[13]	P51
48	D[12]	P52
49	DGND	
50	DGND	

Schematic


Memory + Power Module
Opal Kelly
Opal Kelly Incorporated
Hillsboro, OR 97123
http://www.opalkelly.com

Mechanical Drawing



All dimensions in inches.