Opal Kelly

XEM3001 User's Manual

A business-card sized (3.5'' x 2.0'') experimentation board featuring the Xilinx Spartan 3 FPGA.

The XEM3001 is a small, business-card sized FPGA board featuring the Xilinx Spartan 3 FPGA. Designed as a bare-bones system, the XEM3001 is an excellent experimenting or prototyping system which provides access to nearly all I/O pins on the 208-pin Spartan 3 device. The USB 2.0 interface provides fast downloads and easy access with FrontPanel software. An on-board PLL provides flexible clock generation for a variety of applications and on-board pushbuttons and LEDs allow simple user interfacing when FrontPanel components don't suit the purpose. Dozens of pins at 100-mil spacing are provided and easily fit onto a standard prototyping board with 100-mil hole spacing.

Software, documentation, samples, and related materials are

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Revision History:

Date	Author	Description
20040901	JWJ	Initial release.
20041103	JWJ	Added PLL and JTAG (JP4) connections.

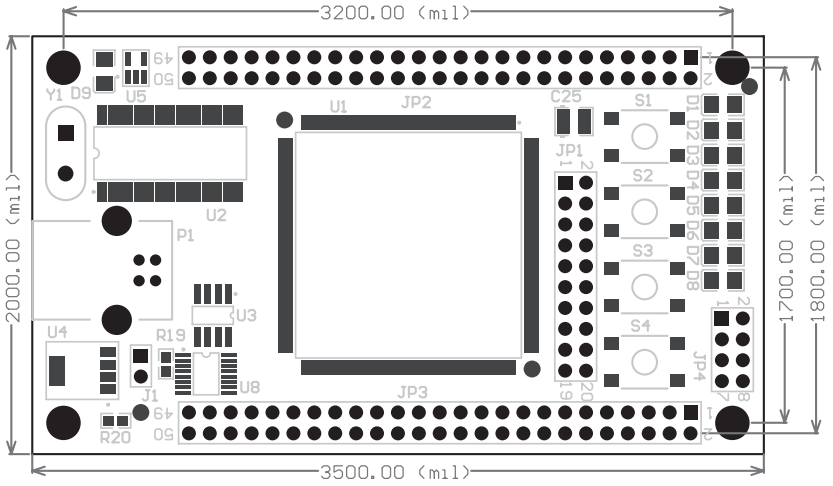
Contents

Introducing the XEM3001

The XEM3001 is a small, business-card sized (3.5'' x 2.0'') FPGA board featuring the Xilinx Spartan 3 FPGA. Designed as a full-featured starter system, the XEM3001 provides access to nearly all I/O pins on the 208-pin Spartan 3 device. The XEM3001 is ideally suited to experiments based on the FrontPanel virtual instrumentation platform, integration into prototype development, or as a quick and easy way to add USB capability to an existing device.

PCB Footprint

A mechanical drawing of the XEM3001 is shown below.



The PCB is 3.5" x 2.0" (88.9mm x 50.8mm) with four mounting holes spaced as shown in the figure. These mounting holes are electrically connected to the ground plane.

The three FPGA-access ports JP1, JP2, and JP3 are located on a 0.1" grid so that the entire board may be attached to a standard prototyping board. The JTAG header JP4, however, is not on this same grid.

Power Supply

The XEM3001 is a bus-powered device in its default configuration (J1 jumper inserted). That is, it takes power from the 5-V USB power and generates the voltages it needs from there. To do so, the XEM3001 has small linear regulators for 3.3-V, 2.5-V, and 1.8-V. External power may be applied to any of the 3.3-V pins on JP1, JP2, or JP3 as long as the J1 jumper is removed. In this case, the 5-V USB power is not used and the device consumes no bus current.

Computers and USB hubs often have USB ports that do not provide bus power. These are called unpowered ports. In order to be operated as a bus-powered device, the XEM3001 must be connected to a USB port that provides bus power. You should check with the hub or computer manufacturer to verify that the port provides bus power.

The XEM3001 may also be self-powered by removing jumper J1. This jumper connects the 3.3-V regulator to the 3.3-V supply plane on the board. By removing this jumper, the 3.3-V supply and therefore the derived 2.5-V and 1.8-V supplies are disconnected from bus power. 3.3 Volts must be supplied externally (either to the device side of the jumper -- the pin closer to the "J1" marking -- or to one of the 3.3-V pins on JP1, JP2, or JP3.

> IMPORTANT NOTE: Under normal operating conditions and with an unconfigured FPGA, the XEM3001 draws approximately 250 mA (170 mA when operating in full-speed on a USB 1.1 port) from the 3.3-V node. FPGA current draw is impossible to predict because it strongly depends on the implemented design and clocking rates. Current requirements of the FPGA can be estimated using Xilinx power estimation tools and should be considered if you think you may be getting close to USB limits. The current can easily be measured by removing the J1 jumper and placing a current meter across the leads. If you need to exceed the 500 mA limit, make sure to apply external power and remove J1.

USB 2.0 Interface

The XEM3001 uses a Cypress CY68013 FX2 USB microcontroller to make the XEM a USB 2.0 peripheral. As a USB peripheral, the XEM is instantly recognized as a plug and play peripheral on millions of PCs. More importantly, FPGA downloads to the XEM happen blazingly fast, virtual instruments under FrontPanel update quickly, and data transfers are much faster than the parallel port interfaces common on many FPGA experimentation boards.

The USB interface also allows the XEM to be bus-powered which means it is ultra-portable requiring just a USB cable and the proper drivers to connect to any supporting PC, including laptops.

On-board Peripherals

The XEM3001 is designed as a low-cost, barebones device. However, a few key peripherals have been added for convenience.

EEPROM

A small serial EEPROM is attached to the USB microcontroller on the XEM3001, but not directly available to the FPGA. The EEPROM is used to store boot code for the microcontroller as well as PLL configuration data and a device identifier string.

The PLL configuration data is loaded from EEPROM and used to reconfigure the PLL each time a new configuration file is loaded to the FPGA. Therefore, stable and active clocks will be present on the FPGA pins as soon as it comes out of configuration. The stored PLL configuration may be changed at any time using FrontPanel's PLL Configuration Dialog.

The EEPROM also stores a device identifier string which may be changed at any time using FrontPanel. The string serves only a cosmetic purpose and is used when multiple XEM devices are attached to the same computer so you may select the proper active device.

Cypress CY22150 PLL

A multi-output, single-VCO PLL can provide up to five clocks, three to the FPGA and another two to the expansion connectors JP2 and JP3. The PLL is driven by a 48-MHz signal output from the USB microcontroller. The PLL can output clocks up to 150-MHz and is configured through the FrontPanel software interface.

LEDs and Pushbuttons

Eight LEDs and four pushbuttons are available for general use as debug inputs and outputs.

Expansion Connectors

Three 0.1"-spaced expansion connectors (JP1, JP2, JP3) are available to connect the XEM to your devices. These connectors provide 3.3v power, ground, PLL outputs, and 88 FPGA pins for general I/O. All expansion connectors are on a 100-mil grid so that the entire XEM can piggy-back onto a standard 100-mil PCB protoboard.

> NOTE: The expansion connectors are not installed at the factory to provide you the flexibility of installing your choice of expansion -- directly soldering wires, or using stacking or right-angle connectors.

FrontPanel Support

The XEM3001 is fully supported by Opal Kelly's FrontPanel software. FrontPanel augments the limited peripheral support with a host of PC-based virtual instruments such as LEDs, hex displays, pushbuttons, toggle buttons, and so on. Essentially, this makes your PC a reconfigurable I/O board and adds enormous value to the XEM3001 as an experimentation or prototyping system.

Programmer's Interface

In addition to complete support within FrontPanel, the XEM3001 is also fully supported by the FrontPanel programmer's interface (API), a powerful C++ class library (and Python wrapper) allowing you to easily interface your own software to the XEM.

Complete documentation and several sample programs are installed with FrontPanel.

FPGA Pin Connections

Host Interface

There are 17 pins that connect the on-board USB microcontroller to the FPGA. These pins comprise the host interface on the FPGA and are used for configuration downloads. After configuration, these pins are used to allow FrontPanel communication with the FPGA.

If the FrontPanel okHostInterface module is instantiated in your design, you must map the interface pins to specific pin locations using Xilinx LOC constraints. This may be done using the Xilinx constraints editor or specifying the constraints manually in a text file. An example is shown below:

Xilinx constraints for okHostInterface pin mappings:

```
NET "hi_clk"      LOC = "P79";
NET "hi_cs"       LOC = "P57";
NET "hi_rdwr"     LOC = "P58";
NET "hi_busy"     LOC = "P81";
NET "hi_irq"      LOC = "P85";
NET "hi_addr<0>"  LOC = "P64";
NET "hi_addr<1>"  LOC = "P63";
NET "hi_addr<2>"  LOC = "P62";
NET "hi_addr<3>"  LOC = "P61";
NET "hi_data<0>"  LOC = "P92";
NET "hi_data<1>"  LOC = "P90";
NET "hi_data<2>"  LOC = "P87";
NET "hi_data<3>"  LOC = "P86";
NET "hi_data<4>"  LOC = "P74";
NET "hi_data<5>"  LOC = "P72";
NET "hi_data<6>"  LOC = "P68";
NET "hi_data<7>"  LOC = "P67";
```

Each of the samples installed with FrontPanel includes a copy of a template constraints file that lists all the XEM3001 pins and maps them to the appropriate FPGA pins using LOC (location) constraints. You can use this template to quickly get the pin locations correct on a new design.

LEDs and Pushbuttons

There are eight LEDs and four pushbuttons on the XEM3001. Each is wired directly to the FPGA as shown in the tables below.

LED	FPGA Pin
D1	205
D2	204
D3	203
D4	200
D5	199
D6	198
D7	197
D8	196

Button	FPGA Pin
BTN1	194
BTN2	191
BTN3	190
BTN4	189

The LED anodes are connected to a pull-up resistor to +3.3VDD and the cathodes wired directly to the FPGA. To turn ON an LED, the FPGA pin should be brought low. To turn OFF an LED, the FPGA pin should be brought high.

The pushbuttons are connected between their respective FPGA pin and DGND. The FPGA side of the connection has a pull-up resistor to +3.3VDD. Therefore, in the pressed state, the FPGA pin will be at DGND (low) and in the unpressed state, the FPGA pin will be at +3.3VDD (high). Note that the pushbuttons are not debounced on the XEM3001. In order to deglitch the signals from the pushbuttons, proper debouncing should be done inside the FPGA.

PLL Connections

The PLL contains six output pins, one of which is left unconnected. The other five are labelled SYS_CLK1 through SYS_CLK5. SYS_CLK4 connects to JP3 and SYS_CLK5 connects to JP2. The other three pins are connected directly to the FPGA. The table below illustrates the PLL connections.

PLL Pin	Clock Name	Connection
LCLK1	SYS_CLK1	FPGA - P80
LCLK2	SYS_CLK2	FPGA - P77
LCLK3	SYS_CLK3	FPGA - P76
LCLK4	SYS_CLK4	JP3 - Pin 48
CLK5	SYS_CLK5	JP2 - Pin 3
CLK6	N/A	

JP4 - JTAG Connector

JP4 is the 8-pin JTAG connector on-board and is connected only to the FPGA. These pins can be connected to an external JTAG command converter (such as the Xilinx JTAG cables) for additional programming capability. The JP4 pins are connected as shown below:

JP4 Pin	Signal
1	+2.5VDD
2	TCK
3	DGND
4	TMS
5	DGND
6	TDI
7	DGND
8	TDO

JP1

JP1 is a 20-pin dual-row 100-mil header, four pins of which are dedicated to power supply. The other 16 pins connect directly to the Spartan 3 on Banks 0 and 1. Pins 17 and 18 of the header connect to global clock pins on the FPGA and can therefore be used as clock inputs to the internal clock network. All 16 FPGA pins may be used as general-purpose input/output.

JP1 Pin	Connection
1	+3.3VDD
2	+3.3VDD
3	I/O 187
4	I/O 185
5	I/O 182
6	I/O 178
7	I/O 176
8	I/O 175
9	I/O 172
10	I/O 171

JP1 Pin	Connection
11	I/O 169
12	I/O 168
13	I/O 167
14	I/O 166
15	I/O 165
16	I/O 162
17	I/O / GCLK6 183
18	I/O / GCLK5 181
19	DGND
20	DGND

JP2

JP2 is a 50-pin dual-row 100-mil header providing access to FPGA Banks 6 and 7. Several pins of this header are dedicated to power supply (+3.3VDD and DGND). Pin 4 of this header is connected to a global clock input on the FPGA and can therefore be used as an input to the global clock network.

Pin 3 on this header is SYSCLK5 and is directly connected to LCLK5 (pin 14) on the Cypress CY22150 PLL. Using FrontPanel's PLL Configuration Dialog, you can configure the clock signal present on this pin.

JP2 Pin	Connection
1	DGND
2	DGND
3	SYS CLK 5
4	I/O / GCLK7 184
5	I/O 5
6	I/O 7
7	I/O 9
8	I/O 10
9	+3.3VDD
10	+3.3VDD
11	I/O 11
12	I/O 12
13	I/O 13
14	I/O 15
15	I/O 16
16	I/O 18
17	I/O 19

JP2 Pin	Connection
18	I/O 20
19	DGND
20	DGND
21	I/O 21
22	I/O 22
23	I/O 24
24	I/O 26
25	I/O 27
26	I/O 28
27	I/O 29
28	I/O 31
29	I/O 33
30	I/O 34
31	DGND
32	DGND
33	I/O 35
34	I/O 36

JP2 Pin	Connection
35	I/O 37
36	I/O 39
37	I/O 40
38	I/O 42
39	I/O 43
40	I/O 44
41	+3.3VDD
42	+3.3VDD
43	I/O 45
44	I/O 46
45	I/O 48
46	I/O 50
47	I/O 51
48	I/O 52
49	DGND
50	DGND

JP3

JP3 is a 50-pin dual-row 100-mil header providing access to FPGA Banks 2 and 3. Several pins of this header are dedicated to power supply (+3.3VDD and DGND). Pin 47 of this header is connected to a global clock input on the FPGA and can therefore be used as an input to the global clock network.

Pin 48 on this header is SYSCLK4 and is directly connected to LCLK4 (pin 12) on the Cypress CY22150 PLL. Using FrontPanel's PLL Configuration Dialog, you can configure the clock signal present on this pin.

JP3 Pin	Connection
1	DGND
2	DGND
3	I/O 156
4	I/O 155
5	I/O 154
6	I/O 152
7	I/O 150
8	I/O 149
9	+3.3VDD
10	+3.3VDD
11	I/O 148
12	I/O 147
13	I/O 146
14	I/O 144
15	I/O 143
16	I/O 141
17	I/O 140

JP3 Pin	Connection
18	I/O 139
19	DGND
20	DGND
21	I/O 138
22	I/O 137
23	I/O 135
24	I/O 133
25	I/O 132
26	I/O 131
27	I/O 130
28	I/O 128
29	I/O 126
30	I/O 125
31	DGND
32	DGND
33	I/O 124
34	I/O 123

JP3 Pin	Connection
35	I/O 122
36	I/O 120
37	I/O 119
38	I/O 117
39	I/O 116
40	I/O 115
41	+3.3VDD
42	+3.3VDD
43	I/O 114
44	I/O 113
45	I/O 111
46	I/O 109
47	I/O / GCLK4 180
48	SYS CLK 4
49	DGND
50	DGND

XEM3001 Quick Reference

JP2 Pin	Connection
1	DGND
2	DGND
3	SYS CLK 5
4	I/O / GCLK7 184
5	I/O 5
6	I/O 7
7	I/O 9
8	I/O 10
9	+3.3VDD
10	+3.3VDD
11	I/O 11
12	I/O 12
13	I/O 13
14	I/O 15
15	I/O 16
16	I/O 18
17	I/O 19
18	I/O 20
19	DGND
20	DGND
21	I/O 21
22	I/O 22
23	I/O 24
24	I/O 26
25	I/O 27
26	I/O 28
27	I/O 29
28	I/O 31
29	I/O 33
30	I/O 34
31	DGND
32	DGND
33	I/O 35
34	I/O 36
35	I/O 37
36	I/O 39
37	I/O 40
38	I/O 42
39	I/O 43
40	I/O 44
41	+3.3VDD
42	+3.3VDD
43	I/O 45
44	I/O 46
45	I/O 48
46	I/O 50
47	I/O 51
48	I/O 52
49	DGND
50	DGND

JP3 Pin	Connection
1	DGND
2	DGND
3	I/O 156
4	I/O 155
5	I/O 154
6	I/O 152
7	I/O 150
8	I/O 149
9	+3.3VDD
10	+3.3VDD
11	I/O 148
12	I/O 147
13	I/O 146
14	I/O 144
15	I/O 143
16	I/O 141
17	I/O 140
18	I/O 139
19	DGND
20	DGND
21	I/O 138
22	I/O 137
23	I/O 135
24	I/O 133
25	I/O 132
26	I/O 131
27	I/O 130
28	I/O 128
29	I/O 126
30	I/O 125
31	DGND
32	DGND
33	I/O 124
34	I/O 123
35	I/O 122
36	I/O 120
37	I/O 119
38	I/O 117
39	I/O 116
40	I/O 115
41	+3.3VDD
42	+3.3VDD
43	I/O 114
44	I/O 113
45	I/O 111
46	I/O 109
47	I/O / GCLK4 180
48	SYS CLK 4
49	DGND
50	DGND

JP1 Pin	Connection
1	+3.3VDD
2	+3.3VDD
3	I/O 187
4	I/O 185
5	I/O 182
6	I/O 178
7	I/O 176
8	I/O 175
9	I/O 172
10	I/O 171
11	I/O 169
12	I/O 168
13	I/O 167
14	I/O 166
15	I/O 165
16	I/O 162
17	I/O / GCLK6 183
18	I/O / GCLK5 181
19	DGND
20	DGND

Host Interface Pin	FPGA Pin
CLK	79
CS	57
RDWR	58
BUSY	81
INT	85
ADDR[3]	61
ADDR[2]	62
ADDR[1]	63
ADDR[0]	64
DATA[7]	92
DATA[6]	90
DATA[5]	87
DATA[4]	86
DATA[3]	74
DATA[2]	72
DATA[1]	68
DATA[0]	67

LED	FPGA Pin
D1	205
D2	204
D3	203
D4	200
D5	199
D6	198
D7	197
D8	196

Button	FPGA Pin
BTN1	194
BTN2	191
BTN3	190
BTN4	189

PLL Pin	Clock Name	Connection
LCLK1	SYS_CLK1	FPGA - P80
LCLK2	SYS_CLK2	FPGA - P77
LCLK3	SYS_CLK3	FPGA - P76
LCLK4	SYS_CLK4	JP3 - Pin 48
CLK5	SYS_CLK5	JP2 - Pin 3
CLK6	N/A