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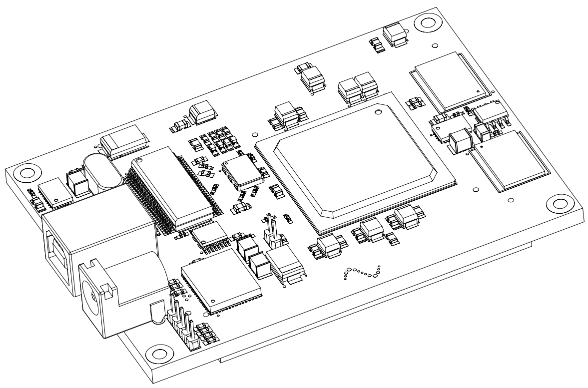

XEM5010 User's Manual

A compact (85mm x 61mm) integration board featuring the Xilinx Virtex-5 FPGA and on-board DDR2 SDRAM, SSRAM, and SPI Flash.

The XEM5010 is a compact USB-based FPGA integration board featuring the Xilinx Virtex-5 FPGA, 256 MB 2x16-bit wide DDR2 SDRAM, 1Mx36 SyncSRAM, 32 Mb non-volatile flash, high-efficiency switching power supplies, and two high-density 0.8-mm expansion connectors. The USB 2.0 interface provides fast configuration downloads and FPGA-PC communication as well as easy access with our popular FrontPanel software and developer's API. An on-board low-jitter, LVDS clock oscillator provides a 100 MHz clock source to the FPGA.

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Revision History:

Date	**Description**
20090721	Initial release.
20090730	Corrected JP2 pins JP2-9, 10, 11, 12.
20090909	Fix typo on pinout page 23. (JP2 relabeled to JP3)
20091105	Updated documentation to include VDC input voltage range and proper location of +3.3v and +1.0v outputs on JP2/JP3.
20091227	Added BRK5010 schematic and mechanical drawing.
20100226	Added BRK5010 errata.
20101101	Added example heatsink part number.
20101104	Added note about on-board termination for the LVDS oscillator.
20110926	Fixed SSRAM pin list.
20140331	Added remark about the Pins reference.
20140812	Fixed typo in I/O voltages section. Can set voltage on six banks (not four).

Contents

Introducing the XEM5010

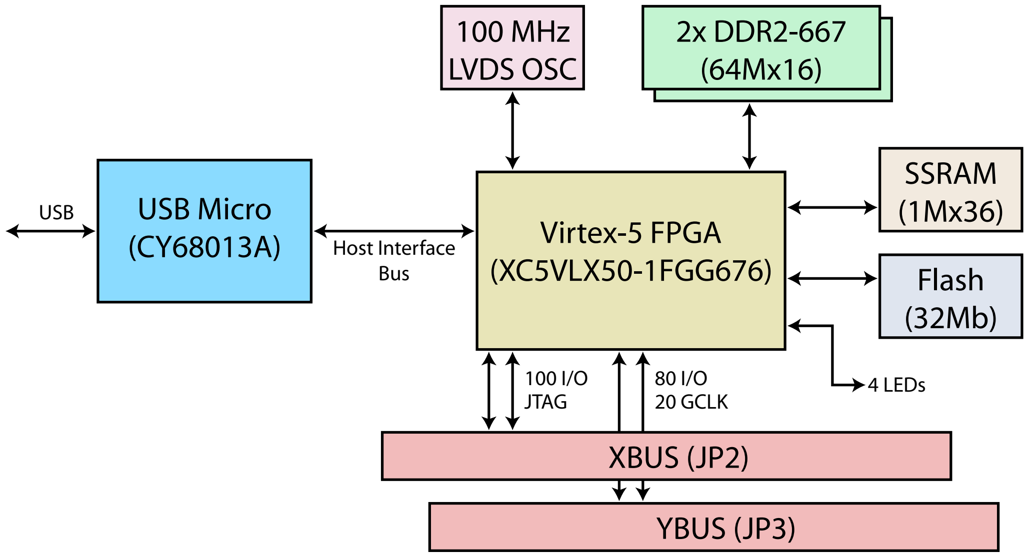
The XEM5010 is a compact (85mm x 61mm, 3.35" x 2.40") FPGA board featuring the Xilinx Virtex-5 FPGA. Designed as a full-featured integration system, the XEM5010 provides access to 200 I/O pins on its 676-pin Virtex-5 device and has 256-MByte of DDR2 SDRAM, 36-Mb of SSRAM, and 4-MByte of Flash memory available to the FPGA.

PCB Footprint

A mechanical drawing of the XEM5010 is shown at the end of this manual. The PCB is 85mm x 61mm with four mounting holes spaced as shown in the figure. These mounting holes are electrically isolated from all signals on the XEM5010. The two connectors (USB and DC power) overhang the PCB by approximately 4mm in order to accomodate mounting within an enclosure.

The XEM5010 has two high-density 120-pin connectors on the bottom side which provide access to many FPGA pins, power, JTAG, and the microcontroller's I2C interface.

Functional Block Diagram



Power Supply

The XEM5010 has four high-efficiency switching regulators to provide clean, well-regulated power to the FPGA and peripherals on the board. These are Enpirion power modules and configured to supply 3.3v, 2.5v, 1.8v, and 1.0v.

P1 is the DC power connector on the board and sources +VDC to all four regulators. Alternatively, +VDC can be provided through the expansion connector (JP3). +VDC must be sourced from a well-regulated power supply in the range of +4.5v to +5.5v.

Supply Heat Dissipation (IMPORTANT!!)

Due to the limited area available on the small form-factor of the XEM5010 and the density of logic provided, heat dissipation should be a concern. This depends entirely on the end application and cannot be predicted in advance by Opal Kelly. Heat sinks may be required on any of the devices on the XEM5010. Of primary focus should be the FPGA (U12). Although the switching supplies are high-efficiency, they are very compact and consume a small amount of PCB area for the current they can provide.

The FPGA will require additional passive or active cooling for even simple designs.

One such passive heatsink would be the INM27002-12PCU/2.6 available from Radian (www.radianheatinks.com). The blue clip version (BU+T710) fits the Virtex-5 on the XEM5010. Of course, this specific heatsink may not be suitable for all designs.

DC Power Connector

The DC power connector on the XEM5010 is part number PJ-102AH from CUI, Inc. It is a standard 2.1mm / 5.5mm power jack. The outer ring is attached to DGND. The center pin is attached to +VDC on expansion connector JP3 as well as the inputs to the switching regulators on the XEM5010.

VBATT

+VBATT is connected to the JP3 expansion connector and can be powered by a daughterboard to the FPGA. This voltage is used to maintain a small memory on the FPGA to support bitstream encryption. Please see the Xilinx Virtex-5 documentation for details.

Supply Currents

The on-board regulators provide the following supplies and respective current:

- +3.3v @ 1.0A - USB microcontroller, clock oscillator, and default FPGA I/O.
- +2.5v @ 2.0A - FPGA VCCAUX
- +1.8v @ 1.0A - DDR2 SDRAM and SSRAM
- +1.0v @ 6.0A - FPGA VCCINT

+3.3v is available on JP2 and +1.0v is available on JP3. Designers should note the current limitations before deciding to use these supplies.

USB Bus Power

The USB 2.0 specification allows for up to 2.5 W (500mA at 5v) to be provided to external peripherals over the USB cable. Due to the potentially high power requirements of the XEM5010, USB power has not been connected. However, the XEM firmware reports to the USB hub as a 500-mA device.

USB 2.0 Interface

The XEM5010 uses a Cypress CY7C68013A FX2LP USB microcontroller to make the XEM a USB 2.0 peripheral. As a USB peripheral, the XEM is instantly recognized as a plug and play peripheral on millions of PCs. More importantly, FPGA downloads to the XEM happen blazingly fast, virtual instruments under FrontPanel update quickly, and data transfers are much faster than the parallel port interfaces common on many FPGA experimentation boards.

On-board Peripherals

The XEM5010 is designed to compactly support a large number of applications with a small number of on-board peripherals. These peripherals are listed below.

Clock Oscillator

The clock oscillator produces a 100 MHz (±50ppm) LVDS signal with 45/55% symmetry and 0.5-ps typical phase jitter (1.0-ps RMS max) measured from 12 kHz - 80 MHz.

Serial EEPROM

A small serial EEPROM is attached to the USB microcontroller on the XEM5010, but not directly available to the FPGA. The EEPROM is used to store boot code for the microcontroller as well as a device identifier string.

The device identifier string may be changed at any time using FrontPanel. The string serves only a cosmetic purpose and is used when multiple XEM devices are attached to the same computer so you may select the proper active device.

256-MByte Synchronous DDR2 DRAM (2x 128-MByte)

The XEM also includes two 128-MByte DDR2 SDRAM with fully independent 16-bit word-wide interfaces to the FPGA. This SDRAMs are attached exclusively to the FPGA and do not share any pins with the expansion connector. The maximum clock rate of the SDRAM is 266 MHz. None of the pins (control, address, or data) are shared between the two SDRAM busses.

The SDRAM is a Micron MT47H64M16HR-3:G (or compatible).

36-Mb Word-Wide Synchronous SRAM

One synchronous SRAM (1M x 36 configuration) is included with dedicated address, data, and control lines routed to the FPGA. The SSRAM is a GSI Technology GS8322Z36GB-200V (or equivalent).

32-Mb SPI Serial Flash

One Numonyx M25P32 (or equivalent) SPI serial flash is connected to the FPGA for non-volatile storage.

LEDs and External LED Connections

Four on-board LEDs are provided for general use. In addition, a 5-pin expansion connector (JP4) allows the connection of a external LEDs. Four pins of this connector are wired to FPGA pins via series 330-Ω resistors.

Expansion Connectors

Two high-density, 120-pin expansion connectors are available on the bottom-side of the XEM5010 PCB. These expansion connectors provide user access to several power rails on the XEM5010, several FPGA clock inputs, the JTAG chain, and 200 non-shared I/O pins on the FPGA.

The connectors on the XEM5010 are Samtec part number: QSE-060-01-F-D-A. The table below lists the appropriate Samtec mating connectors along with the total mated height.

Samtec Part Number	Mated Height
QTE-060-01-F-D-A	5.00mm (0.198")
QTE-060-02-F-D-A	8.00mm (0.316")

FrontPanel Support

The XEM5010 is fully supported by Opal Kelly's FrontPanel software. FrontPanel augments the limited peripheral support with a host of PC-based virtual instruments such as LEDs, hex displays, pushbuttons, toggle buttons, and so on. Essentially, this makes your PC a reconfigurable I/O board and adds enormous value to the XEM5010 as an experimentation or prototyping system.

Programmer's Interface

In addition to complete support within FrontPanel, the XEM5010 is also fully supported by the FrontPanel programmer's interface (API), a powerful C++ class library available to Windows and Linux programmers allowing you to easily interface your own software to the XEM.

In addition to the C++ library, wrappers have been written for C#, Java, Python, and Ruby making the API available under those languages as well. Sample wrappers are also provided for Matlab and LabVIEW.

Complete documentation and several sample programs are installed with FrontPanel.

Applying the XEM5010

Host Interface

There are 26 pins that connect the on-board USB microcontroller to the FPGA. These pins comprise the host interface on the FPGA and are used for configuration downloads. After configuration, these pins are used to allow FrontPanel communication with the FPGA.

If the FrontPanel okHost module is instantiated in your design, you must map the interface pins to specific pin locations using Xilinx LOC constraints. This may be done using the Xilinx constraints editor or specifying the constraints manually in a text file. An example is shown below:

Xilinx constraints for okHost pin mappings:

```
NET "hi_in<0>"      LOC="AD13" | IOSTANDARD="LVCMOS33";
NET "hi_in<1>"      LOC="AD15" | IOSTANDARD="LVCMOS33";
NET "hi_in<2>"      LOC="AD14" | IOSTANDARD="LVCMOS33";
NET "hi_in<3>"      LOC="AB12" | IOSTANDARD="LVCMOS33";
NET "hi_in<4>"      LOC="Y8"   | IOSTANDARD="LVCMOS33";
NET "hi_in<5>"      LOC="AA8"  | IOSTANDARD="LVCMOS33";
NET "hi_in<6>"      LOC="AA17" | IOSTANDARD="LVCMOS33";
NET "hi_in<7>"      LOC="AB17" | IOSTANDARD="LVCMOS33";
NET "hi_out<0>"     LOC="AC14" | IOSTANDARD="LVCMOS33";
NET "hi_out<1>"     LOC="AC11" | IOSTANDARD="LVCMOS33";
NET "hi_inout<0>"   LOC="AD18" | IOSTANDARD="LVCMOS33";
NET "hi_inout<1>"   LOC="AC18" | IOSTANDARD="LVCMOS33";
NET "hi_inout<2>"   LOC="AB10" | IOSTANDARD="LVCMOS33";
NET "hi_inout<3>"   LOC="AB9"  | IOSTANDARD="LVCMOS33";
NET "hi_inout<4>"   LOC="AC17" | IOSTANDARD="LVCMOS33";
NET "hi_inout<5>"   LOC="AC16" | IOSTANDARD="LVCMOS33";
NET "hi_inout<6>"   LOC="AC8"  | IOSTANDARD="LVCMOS33";
NET "hi_inout<7>"   LOC="AC9"  | IOSTANDARD="LVCMOS33";
NET "hi_inout<8>"   LOC="Y12"  | IOSTANDARD="LVCMOS33";
NET "hi_inout<9>"   LOC="Y13"  | IOSTANDARD="LVCMOS33";
NET "hi_inout<10>"  LOC="AA15" | IOSTANDARD="LVCMOS33";
NET "hi_inout<11>"  LOC="AB14" | IOSTANDARD="LVCMOS33";
NET "hi_inout<12>"  LOC="AA12" | IOSTANDARD="LVCMOS33";
NET "hi_inout<13>"  LOC="AB11" | IOSTANDARD="LVCMOS33";
NET "hi_inout<14>"  LOC="AA13" | IOSTANDARD="LVCMOS33";
NET "hi_inout<15>"  LOC="AA14" | IOSTANDARD="LVCMOS33";
NET "hi_muxsel"     LOC="AB15" | IOSTANDARD="LVCMOS33";
```

Each of the samples installed with FrontPanel includes a copy of a template constraints file that lists all the XEM5010 pins and maps them to the appropriate FPGA pins using LOC (location) constraints. You can use this template to quickly get the pin locations correct on a new design.

MUXSEL

MUXSEL is a signal on the XEM5010 which selects the signal path to the FPGA programming signals D0 and CCLK. When low (deasserted), the FPGA and USB microcontroller are connected. When high (asserted), the FPGA and PROM are connected.

In normal USB-programmed operation, J1 pulls MUXSEL low, connecting the FPGA and USB microcontroller at all times. This allows USB-based programming of the FPGA and subsequent USB communication with the FPGA design after configuration.

In order to allow the PROM to configure the FPGA, J1 must be removed. However, if the USB is to communicate with the FPGA post-configuration, MUXSEL must be deasserted. Therefore, the FPGA outputs MUXSEL so that, post-configuration, the FPGA can deassert MUXSEL and communicate over USB even after the PROM has configured it.

The end result is that your FPGA design should tie HI_MUXSEL to 0. For example, in Verilog:

```
assign hi_muxsel = 1'b0;
```

LEDs

There are four LEDs and four external LED pins on the XEM5010. Each is wired directly to the FPGA according to the pin mapping tables at the end of this document.

The LED anodes are connected to a pull-up resistor to +3.3VDD and the cathodes wired directly to the FPGA. To turn ON an LED, the FPGA pin should be brought low. To turn OFF an LED, the FPGA pin should be brought high.

The external LED connector is wired a bit differently. JP4-1 is attached to +3.3VDD. JP4-2 through JP4-5 are each attached through a 330-Ω resistor to an FPGA pin. Externally, you should connect the four LED anodes to JP4-1 (+3.3VDD). The four cathode should be attached to the other pins on JP4.

Clock Oscillator Connections

The LVDS clock oscillator produces a 100 MHz LVDS signal which is presented on FPGA pins AD8 and AC7. These are L4P_GC_4 and L4N_GC4 inputs, respectively. An on-board 100-ohm termination resistor is present.

JTAG

On the XEM5010, the FPGA is the only device on the JTAG chain. The JTAG pins connecting to the FPGA are available on the expansion connector JP2 so that you can attach a suitable JTAG chain or programmer on your boart.

SPI Flash Connections

The on-board SPI flash device is attached to the FPGA according to the following table.

Flash Pin	Signal
CLK	AA18
CS	AA10
DOUT	Y18
DIN	AA9

FPGA Configuration via SPI Flash

The Virtex-5 on the XEM5010 may be configured by USB or SPI Flash. When using USB, the FPGA may be configured at any time. When booting by SPI Flash, configuration takes place at power-on. To boot to the configuration file loaded into the SPI Flash, remove the jumper at J1.

To load the SPI Flash with your configuration data, we have provided a sample (FlashLoader) which is located in the Samples directory of your installation. This is a simple command-line utility that can be used to transfer a configuration bitfile to SPI Flash. The source code to the software is included so you can include this utility in your own application, if required.

DDR2 SDRAM

FPGA Connections

The DDR2 SDRAMs are connected exclusively to the 1.8v I/O on Banks 11, 12, 15, and 16 of the FPGA. The tables below list these connections. DDR2A is U15 on the PCB. DDR2B is U14.

DDR2A Pin	FPGA Pin
CK	D5
$\overline{\text{CK}}$	D6
CKE	H6
$\overline{\text{CS}}$	F4
$\overline{\text{RAS}}$	G6
$\overline{\text{CAS}}$	G7
$\overline{\text{WE}}$	F5
LDQS	D8
$\overline{\text{LDQS}}$	C8
UDQS	B7
$\overline{\text{UDQS}}$	A7
LDM	C13
UDM	A9
ODT	J6
A0	E7
A1	B2
A2	B1
A3	C1
A4	D1
A5	A3
A6	A2
A7	C3
A8	C2

DDR2A Pin	FPGA Pin
A9	B4
A10	C4
A11	C7
A12	C6
BA0	E5
BA1	E6
BA2	F7
D0	D11
D1	D10
D2	C11
D3	C12
D4	B12
D5	A13
D6	A12
D7	C9
D8	B9
D9	B10
D10	B11
D11	A10
D12	A8
D13	B5
D14	B6
D15	D3

DDR2B Pin	FPGA Pin
CK	D21
$\overline{CK}$	D20
CKE	H21
$\overline{CS}$	F23
$\overline{RAS}$	E22
$\overline{CAS}$	E23
$\overline{WE}$	F22
LDQS	A20
$\overline{LDQS}$	B20
UDQS	C19
$\overline{UDQS}$	D19
LDM	B15
UDM	B19
ODT	G21
A0	G20
A1	D25
A2	D26
A3	C26
A4	B26
A5	A25
A6	B25
A7	C24
A8	D24

DDR2B Pin	FPGA Pin
A9	C23
A10	B24
A11	B21
A12	C21
BA0	E20
BA1	E21
BA2	F20
D0	C14
D1	B14
D2	A14
D3	A15
D4	B16
D5	D16
D6	C16
D7	D18
D8	B17
D9	A17
D10	A18
D11	A19
D12	C18
D13	B22
D14	A22
D15	A23

Cascaded DCI

The FPGA interface to the DDR2 SDRAM utilizes the digitally-controlled impedance (DCI) feature of the Virtex-5. VRN and VRP pads on banks 15 and 16 are attached through 1% 49.9Ω resistors to +1.8VDD and DGND, respectively. Banks 11 and 12 use references that are "cascaded" from banks 15 and 16.

Cascade configuration must be specified in your constraints file (.UCF). For example:

```
CONFIG DCI_CASCADE = “16 12”;
CONFIG DCI_CASCADE = “15 11”;
```

Memory Interface Generator (MIG)

MIG is part of the Xilinx Core Generator and can be used to create a DDR2 memory controller for the XEM5010. You should read and become familiar with the DDR2 SDRAM datasheet as well as MIG and the core datasheet. Although MIG can save a tremendous amount of development time, understanding all this information is critical to building a working DDR2 memory interface.

MIG Settings

The following are the settings used to generate the MIG core for our RAMTester sample using Xilinx Core Generator. These settings were used with ISE 10.2 and MIG 2.3. Note that settings may be slightly different for different versions of ISE or MIG.

Frequency	266 MHz	
Memory Type	Component	
Memory Part	MT47H64M16XX-3 (1Gb, x16)	
Data Width	16	
Data Mask	Checked	
Burst Length	4(010)	[default]
Burst Type	Sequential(0)	[default]
CAS Latency	4(100)	[default]
Output drive strength	Reducedstrength(1)	
RTT(nominal)	75ohms(01)	[default]
Additive latency(AL)	0(000)	[default]
Use DCM	Your option	
DCI for DQ/DQS	CHECKED	
DCI for address/control	CHECKED	
Class for address/control	Class II	
Debug signals	Your option	
Limit to 2 bytes per bank	No	
System clock	Differential	

MIG Pin Selection

To help MIG select the proper pins for the constraints (UCF), you can direct it to reserve non-DDR2 banks and tell it where to map controllers for the others. The selection process is:

- Reserve banks 1, 2, 3, 13, 14, 17, 18, 21. MIG will not use these.
- For controller C0, check all in banks 4, 12, 16. Uncheck all others.
- For controller C1, check all in banks 4, 11, 15. Uncheck all others.

Synchronous SRAM

The SSRAM has a full 36-bit wide data bus (4 bytes + 4 parity pits). The CLK pin is attached directly to the FPGA with the intent that the FPGA provide a synchronous clock in the so-called "source synchronous" manner. This helps align clock and data between the FPGA and SSRAM.

The redundant chip enable pins of the SSRAM have been tied to enable, as appropriate. E2 is tied to +1.8VDD and $\overline{\text{E3}}$ is tied to DGND. ZQ has been left as a no-connect. $\overline{\text{LBO}}$ is tied to DGND, enabling linear byte order operation. Finally, all four byte enables ($\overline{\text{BA}}$, $\overline{\text{BB}}$, $\overline{\text{BC}}$, and $\overline{\text{BD}}$) are tied to DGND.

High-Performance Operation

The SSRAM can achieve operation to 200 MHz, but requires careful consideration of all FPGA timing parameters. We provide the following as suggestions based on our development of test code, but recommend a thorough timing analysis to achieve high-performance, reliable operation. A good understanding of the SSRAM and FPGA timing datasheets is critical to this analysis.

The SSRAM has a 0.5-ns hold time. By setting the SSRAM_CLK output from the FPGA to "FAST", this can advance the timing of the CLK in comparison to the address/control lines. According to the FPGA timings (T_{IOOP}), this achieves approximately 0.6-ns hold time.

Delays from FPGA pads to the internal fabric can be significant and cause problems at high clock rates. You must consider all delays when determining timing. The following illustrates the timings considered for SSRAM reads. Note that parts will differ depending on manufacturing process corners and operating techniques. Adaptive techniques using the IDELAY elements help achieve optimal results.

T_{OCKQ}	OLOGIC CLK-to-OQ	0.62 ns
T_{IOOP}	Delay from O pin to the IOB pad for CLOCK output	1.93 ns
T_{KQ}	SSRAM clock to Q (read timing)	5.00 ns
T_{IOPI}	Delay from IOB pad to the I pin of the IOB	0.89 ns
T_{IDOCK}	ILOGIC D pin setup with respect to CLK without delay	0.39 ns
	Total	8.83 ns

This table indicates that for clock frequencies exceeding approximately 113 MHz, SSRAM data reads may not be available to the FPGA fabric until the next clock cycle. Therefore, there is a single-cycle read delay inherent in the design routing that must be accounted for in your design.

SSRAM / FPGA Connections

SSRAM Pin	FPGA Pin
CLK	R22
$\overline{\text{CKE}}$	L4
$\overline{\text{WE}}$	J21
$\overline{\text{CE1}}$	M22
$\overline{\text{OE}}$	K22
ADV/$\overline{\text{LD}}$	J5
ZZ	K5
$\overline{\text{FT}}$	M6
A0	L5
A1	M5
A2	M4
A3	L3
A4	J4
A5	H4
A6	G4
A7	P3
A8	N4
A9	T3
A10	R3
A11	H19
A12	K20
A13	P19

SSRAM Pin	FPGA Pin
A14	R23
A15	J23
A16	N23
A17	L23
A18	K23
A19	H23
A20	P23
D0	R7
D1	R5
D2	P4
D3	R6
D4	P6
D5	N6
D6	P5
D7	M7
DP1	N7
D8	M19
D9	L20
D10	M21
D11	P20
D12	N21
D13	P21

SSRAM Pin	FPGA Pin
D14	N22
D15	L22
DP2	L19
D16	H9
D17	G11
D18	G10
D19	H11
D20	G12
D21	H12
D22	F13
D23	H13
DP3	G9
D24	G14
D25	H14
D26	G15
D27	F15
D28	H17
D29	G17
D30	G16
D31	G19
DP4	H18

Expansion Connectors

Opal Kelly Pins is an interactive online reference for the expansion connectors on all Opal Kelly FPGA integration modules. It provides additional information on pin capabilities, pin characteristics, and PCB routing. Additionally, Pins provides a tool for generating constraint files for place and route tools. Pins can be found at the URL below.

http://www.opalkelly.com/pins

IMPORTANT NOTE: 3.3v I/O Operation

As process technology shrinks, I/O voltages tend lower. The Xilinx Virtex-5 FPGA is no exception and has limited 3.3v I/O operation. Before using the XEM5010 to interface to any 3.3v design, please review the *Xilinx Virtex-5 FPGA User Guide*, Chapter 6: 3.3V I/O Design Guidelines.

JP2

JP2 is a 120-pin high-density connector providing access to FPGA Banks 13, 17, and 21.

Pin mappings for JP2 are listed at the end of this document in the "Quick Reference" section. For each JP2 pin, the corresponding board connection is listed. For pins connected to the FPGA, the corresponding FPGA pin number is also shown. Finally, for pins routed to differential pair I/Os on the FPGA, the FPGA signal names and routed track lengths have been provided to help you equalize lengths on differential pairs.

JP3

JP3 is a 120-pin high-density connector providing access to FPGA Banks 14, 18, and 3. Bank 3 is primarily a clock-input bank providing up to 10 differential clock inputs or 20 single-ended inputs.

Pin mappings for JP3 are listed at the end of this document in the "Quick Reference" section. For each JP3 pin, the corresponding board connection is listed. For pins connected to the FPGA, the corresponding FPGA pin number is also shown. Finally, for pins routed to differential pair I/Os on the FPGA, the FPGA signal names and routed track lengths have been provided to help you equalize lengths on differential pairs.

Setting I/O Voltages

The Virtex-5 FPGA allows users to set I/O bank voltages in order to support several different I/O signalling standards. This functionality is supported by the XEM5010 by allowing the user to connect independent supplies to the FPGA VCCO pins on six of the FPGA banks.

By default, ferrite beads have been installed which attach each VCCO bank to the +3.3VDD supply. If you intend to supply power to a particular I/O bank, you MUST remove the appropriate ferrite beads. Power can then be supplied through the expansion connectors.

The table below lists details for user-supplied I/O bank voltages.

I/O Bank	Expansion Pin	FPGA Pins	Ferrite Bead
3	JP3-2, JP3-4	E14, D17	FB5

I/O Bank	Expansion Pin	FPGA Pins	Ferrite Bead
13	JP2-1, JP2-3	N20, M23, R24	FB1
14	JP3-41, JP3-43	W2, R4, V5	FB2
17	JP2-42, JP2-44	T21, W22, V25	FB3
18	JP3-85, JP3-87	AB3, AA6, AD7	FB4
21	JP2-86, JP2-88	AC20, AB23, AE24	FB6

Considerations for Differential Signals

The XEM5010 PCB layout and routing has been designed with several applications in mind, including applications requiring the use of differential (LVDS) pairs. Please refer to the Xilinx Virtex-5 datasheet for details on using differential I/O standards with the Virtex-5 FPGA.

FPGA I/O Bank Voltages

In order to use differential I/O standards with the Virtex-5, you must set the VCCO voltages for the appropriate banks to 2.5v according to the Xilinx Virtex-5 datasheet. Please see the section above entitled "Setting I/O Voltages" for details.

Characteristic Impedance

The characteristic impedance of all routes from the FPGA to the expansion connector is 50-Ω.

Differential Pair Lengths

In many cases, it is desirable that the route lengths of a differential pair be matched within some specification. Care has been taken to route differential pairs on the FPGA to adjacent pins on the expansion connectors whenever possible. We have also included the lengths of the board routes for these connections to help you equalize lengths in your final application. Due to space constraints, some pairs are better matched than others.

Digitally Controlled Impedance (DCI)

The Xilinx Virtex-5 supports digitally controlled impedance. This functionality is supported when precision resistors are connected externally between the FPGA VRN/VRP lines and +VCCO/DGND, respectively. These FPGA pins have been routed to the expansion connectors so that you may add resistors, as appropriate, on your daughterboard.

BRK5010 Breakout Board

The BRK5010 is a simple breakout board for the XEM5010 that conducts the high-density JP2 and JP3 signals to 2-mm headers for probing and simple prototyping. The board also serves as a reference design for boards to attach to the module. The mechanical drawing for this board is shown at the end of this document.

JP1 on the BRK5010 is a JTAG header compatible with the 2-mm Xilinx JTAG programming cables. JP2A/B/C are directly attached to the mating JP2 connector on the XEM5010. JP3A/B/C are directly attached to the mating JP3 connector on the XEM5010. The connections are straightforward: Pin 1 of JP2 (JP2-1) connects to JP2A-1. JP2-2 connects to JP2A-2. JP2-120 connects to JP2A-120.

Errata: Datecode 20091013

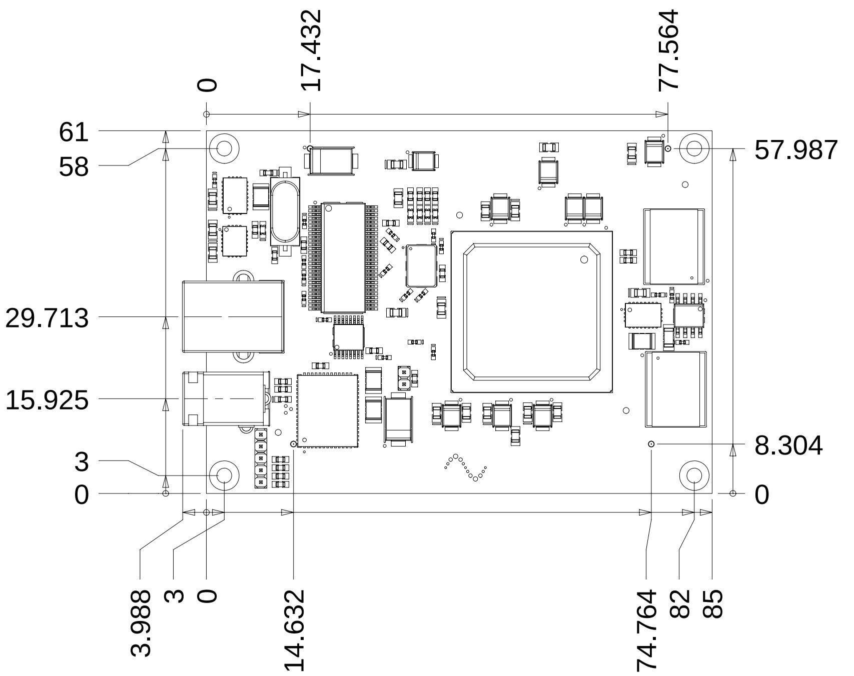
BRK5010 boards with PCB datecode 20091013 have the XEM5010 mounting holes incorrectly inset by 0.5mm. The Samtec connectors (JP2 and JP3) are correctly placed. This error is corrected with PCB datecode 20091209 as shown in the mechanical drawing.

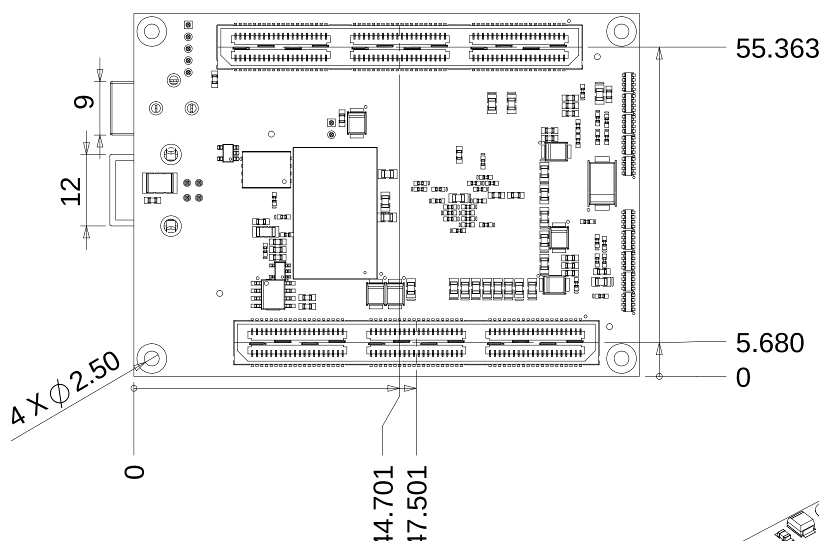
Errata: Datecode 20091013 and 20091209

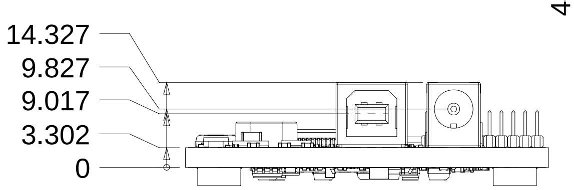
BRK5010 boards with PCB datecode 20091013 and 20091209 have incorrect routing as follows. Two pins were mis-routed, causing subsequent pins to be disjoint.

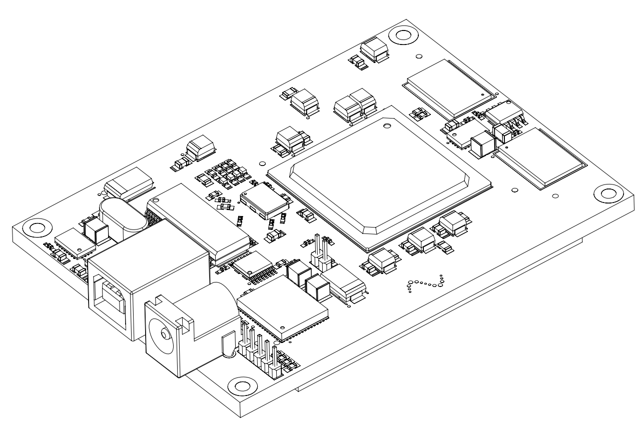
JP2 Samtec	2mm Pin Connection
JP2-86	JP2-86
JP2-88	JP2-88
JP2-90	NOT CONNECTED
JP2-92	NOT CONNECTED
JP2-94	JP2C-90
JP2-96	JP2C-92
JP2-98	JP2C-94
JP2-100	JP2C-96
JP2-102	JP2C-98
JP2-104	JP2C-100
JP2-106	JP2C-102
JP2-108	JP2C-104

XEM5010 Mechanical Drawing





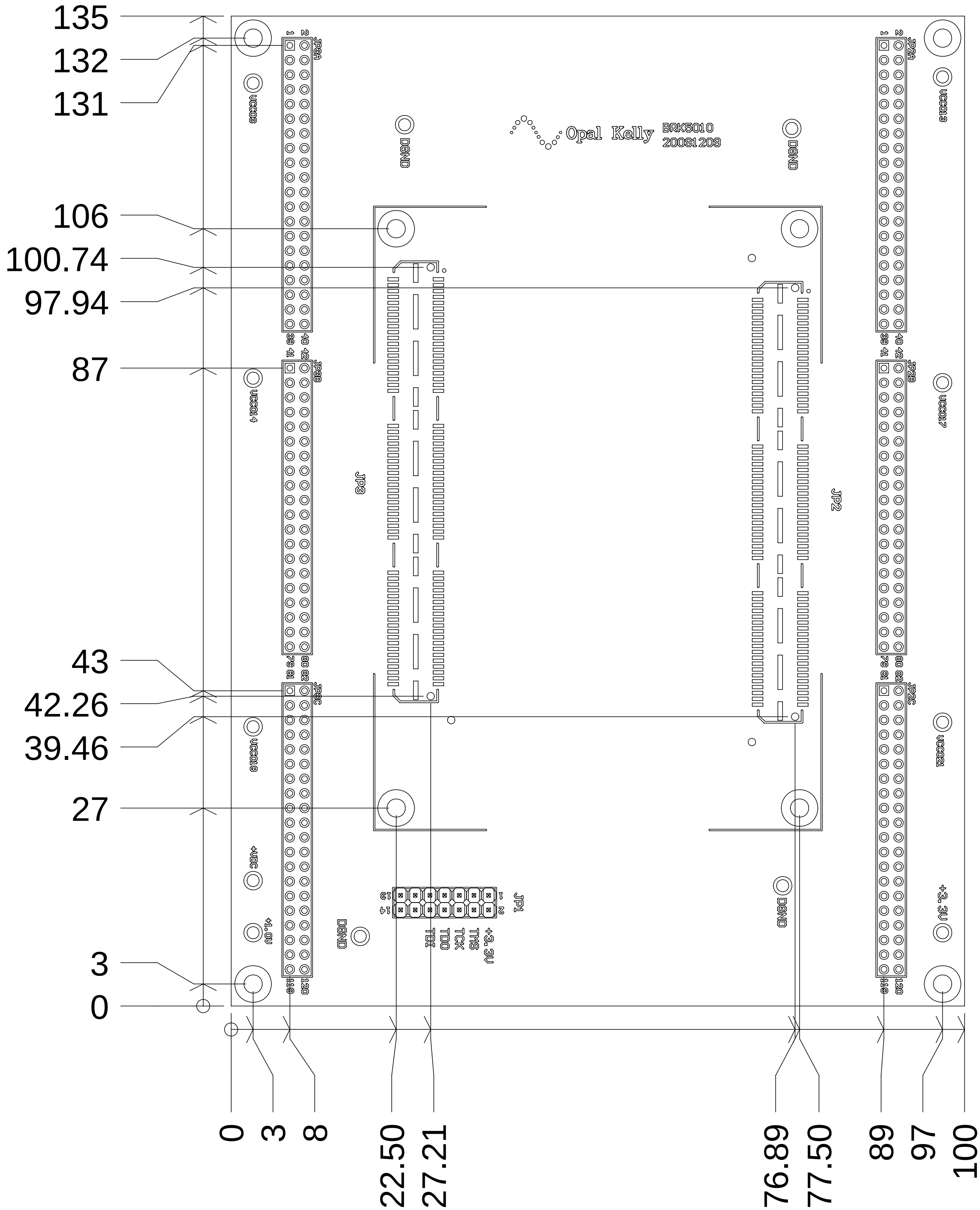




All dimensions in mm.

BRK5010 Mechanical Drawing

All dimensions in mm.



BRK5010 Schematic (20100226)

XEM5010 Quick Reference

JP2 Pin	Connection	FPGA LVDS	Length (mm)
1	VCCO13		
3	VCCO13		
5	E25	L1P_SM7P_13	23.645
7	E26	L1N_SM7N_13	23.253
9	G24	L3P_SM5P_13	21.779
11	G25	L3N_SM5N_13	21.616
13	H24	L5P_SM4P_13	23.678
15	J24	L5N_SM4N_13	23.678
17	K25	L7P_SM2P_13	19.447
19	K26	L7N_SM2N_13	19.558
21	M24	L9P_CC_SM0P_13	23.999
23	N24	L9N_CC_SM0N_13	24.009
25	P25	L11P_CC_13	21.800
27	P24	L11N_CC_13	21.825
29	T24	L13P_13	25.905
31	T25	L13N_13	25.992
33	U24	L15P_13	27.261
35	U25	L15N_13	26.814
37	Y25	L17P_13	30.170
39	Y26	L17N_13	30.139
41	AC26	L19P_13	27.374
43	AB26	L19N_13	27.494
45	T23	L0P_17	24.936
47	T22	L0N_17	25.030
49	T20	L2P_17	23.799
51	T19	L2N_17	23.861
53	W24	L4P_17	23.640
55	W23	L4N_VREF_17	23.730
57	AA23	L6P_17	19.372
59	AA24	L6N_17	19.263
61	AC23	L8P_CC_17	24.382
63	AC22	L8N_CC_17	24.462
65	AB22	L10P_CC_17	26.078
67	AA22	L10N_CC_17	26.134
69	V21	L12P_VRN_17	30.810
71	V22	L12N_VRP_17	30.914
73	U19	L14P_17	29.055
75	U20	L14N_VREF_17	28.799
77	Y21	L16P_17	33.480
79	Y20	L16N_17	33.372
81	AB20	L18P_17	51.300
83	AB19	L18N_17	51.130
85	AD24	L0P_21	25.449
87	AD23	L0N_21	25.267
89	AF24	L2P_21	27.536
91	AF25	L2N_21	27.395
93	AF23	L4P_21	31.210
95	AE23	L4N_VREF_21	31.219
97	AE20	L6P_21	33.467
99	AE21	L6N_21	32.951

JP2 Pin	Connection	FPGA LVDS	Length (mm)
101	AF19	L9P_CC_21	34.414
103	AF20	L9N_CC_21	34.361
105	-		
107	-		
109	-		
111	-		
113	JTAG_TDI		
115	JTAG_TDO		
117	+3.3VDD		
119	+3.3VDD		

Host Interface Pin	FPGA Pin
HI_IN[0]	AD13
HI_IN[1]	AD15
HI_IN[2]	AD14
HI_IN[3]	AB12
HI_IN[4]	Y8
HI_IN[5]	AA8
HI_IN[6]	AA17
HI_IN[7]	AB17
HI_OUT[0]	AC14
HI_OUT[1]	AC11
HI_INOUT[0]	AD18
HI_INOUT[1]	AC18
HI_INOUT[2]	AB10
HI_INOUT[3]	AB9
HI_INOUT[4]	AC17
HI_INOUT[5]	AC16
HI_INOUT[6]	AC8
HI_INOUT[7]	AC9
HI_INOUT[8]	Y12
HI_INOUT[9]	Y13
HI_INOUT[10]	AA15
HI_INOUT[11]	AB14
HI_INOUT[12]	AA12
HI_INOUT[13]	AB11
HI_INOUT[14]	AA13
HI_INOUT[15]	AA14
HI_MUXSEL	AB15

LED	FPGA Pin
D2	AD10
D3	AC12
D4	AD11
D5	AC13

Ext LED	FPGA Pin
JP4-2	AE17
JP4-3	AF17
JP4-4	AE16
JP4-5	AF14

XEM5010 Quick Reference

JP2 Pin	Connection	FPGA LVDS	Length (mm)
2	F24	L0P_SM8P_13	17.920
4	F25	L0N_SM8N_13	17.945
6	G26	L2P_SM6P_13	18.878
8	H26	L2N_SM6N_13	19.233
10	J25	L4P_13	18.172
12	J26	L4N_VREF_13	18.310
14	L24	L6P_SM3P_13	21.319
16	L25	L6N_SM3N_13	21.635
18	M25	L8P_CC_SM1P_13	18.474
20	M26	L8N_CC_SM1N_13	18.465
22	P26	L10P_CC_13	19.364
24	N26	L10N_CC_13	19.620
26	R25	L12P_VRN_13	16.344
28	R26	L12N_VRP_13	16.286
30	V26	L14P_13	21.300
32	U26	L14N_VREF_13	21.440
34	W25	L16P_13	17.332
36	W26	L16N_13	17.317
38	AB25	L18P_13	20.699
40	AA25	L18N_13	20.744
42	VCCO17		
44	VCCO17		
46	R21	L1P_17	19.861
48	R20	L1N_17	20.027
50	U22	L3P_17	15.545
52	U21	L3N_17	15.717
54	V24	L5P_17	16.826
56	V23	L5N_17	17.110
58	Y23	L7P_17	15.857
60	Y22	L7N_17	15.963
62	AB24	L9P_CC_17	17.127
64	AC24	L9N_CC_17	16.869
66	AC21	L11P_CC_17	17.567
68	AB21	L11N_CC_17	17.766
70	W21	L13P_17	22.734
72	W20	L13N_17	23.333
74	V19	L15P_17	25.259
76	W19	L15N_17	25.277
78	AD19	L17P_17	27.793
80	AC19	L17N_17	27.884
82	AA20	L19P_17	29.285
84	AA19	L19N_17	29.034
86	VCCO21		
88	VCCO21		
90	AE26	L1P_21	27.294
92	AD26	L1N_21	27.552
94	AE25	L3P_21	25.709
96	AD25	L3N_21	25.941
98	AD20	L5P_21	31.507
100	AD21	L5N_21	31.433

JP2 Pin	Connection	FPGA LVDS	Length (mm)
102	AF18	L8P_CC_21	30.297
104	AE18	L8N_CC_21	30.250
106	AF15	L12P_VRN_21	39.562
108	AE15	L12N_VRP_21	36.649
110	-		
112	-		
114	JTAG_TCK		
116	JTAG_TMS		
118	-		
120	EXT_PROG		

XEM5010 Quick Reference

JP3 Pin	Connection	FPGA LVDS	Length (mm)
1	D13	L1P_CC_GC_3	33.243
3	D14	L1N_CC_GC_3	33.452
5	D15	L3P_GC_3	31.635
7	E15	L3N_GC_3	33.008
9	E16	L5P_GC_3	32.911
11	E17	L5N_GC_3	36.610
13	E18	L7P_GC_3	34.778
15	F19	L7N_GC_3	36.686
17	F18	L9P_GC_3	34.093
19	F17	L9N_GC_3	33.077
21	E2	L0P_14	12.054
23	E1	L0N_14	12.088
25	G1	L2P_14	14.327
27	H1	L2N_14	14.562
29	K3	L4P_14	16.062
31	K2	L4N_VREF_14	15.936
33	L2	L6P_14	16.838
35	K1	L6N_14	16.746
37	M1	L8P_CC_14	11.548
39	N1	L8N_CC_14	11.549
41	VCCO14		
43	VCCO14		
45	P1	L10P_CC_14	9.879
47	R1	L10N_CC_14	9.808
49	U2	L12P_VRN_14	14.723
51	U1	L12N_VRP_14	14.815
53	Y1	L14P_14	12.271
55	W1	L14N_VREF_14	12.325
57	AB2	L16P_14	15.090
59	AB1	L16N_14	14.949
61	AE1	L18P_14	13.076
63	AD1	L18N_14	13.151
65	V3	L0P_18	20.001
67	U4	L0N_18	20.156
69	T7	L2P_18	21.430
71	U7	L2N_18	21.431
73	V4	L4P_18	20.349
75	W4	L4N_VREF_18	20.396
77	V6	L6P_18	23.772
79	V7	L6N_18	23.646
81	Y6	L8P_CC_18	26.348
83	Y5	L8N_CC_18	26.439
85	VCCO18		
87	VCCO18		
89	Y7	L10P_CC_18	29.135
91	AA7	L10N_CC_18	29.099
93	AC4	L12P_VRN_18	26.872
95	AC3	L12N_VRP_18	27.008
97	AB6	L14P_18	30.749
99	AB5	L14N_VREF_18	30.881

JP3 Pin	Connection	FPGA LVDS	Length (mm)
101	AF3	L16P_18	25.748
103	AE3	L16N_18	25.596
105	AF5	L18P_18	32.149
107	AF4	L18N_18	32.020
109	-		
111	-		
113	USB_SCL		
115	+VBATT		
117	+1.0VDD		
119	+1.0VDD		

XEM5010 Quick Reference

JP3 Pin	Connection	FPGA LVDS	Length (mm)
2	VCCO3		
4	VCCO3		
6	F8	L8P_GC_3	29.217
8	E8	L8N_GC_3	29.318
10	F9	L6P_GC_3	34.803
12	F10	L6N_GC_3	34.662
14	E10	L4P_GC_3	38.438
16	E11	L4N_GC_VREF_3	38.546
18	E12	L2P_GC_VRN_3	31.833
20	F12	L2N_GC_VRP_3	31.838
22	F14	L0P_CC_GC_3	31.884
24	E13	L0N_CC_GC_3	31.705
26	F3	L1P_14	26.258
28	E3	L1N_14	25.904
30	F2	L3P_14	20.002
32	G2	L3N_14	19.996
34	H3	L5P_14	23.268
36	J3	L5N_14	23.276
38	J1	L7P_14	18.790
40	H2	L7N_14	18.999
42	M2	L9P_CC_14	20.953
44	N2	L9N_CC_14	20.999
46	T2	L11P_CC_14	20.336
48	R2	L11N_CC_14	20.552
50	V2	L13P_14	20.935
52	V1	L13N_14	20.812
54	AA2	L15P_14	19.339
56	Y2	L15N_14	19.314
58	AC2	L17P_14	22.247
60	AC1	L17N_14	22.021
62	AF2	L19P_14	20.487
64	AE2	L19N_14	20.412
66	T5	L1P_18	28.568
68	T4	L1N_18	28.262
70	U5	L3P_18	24.062
72	U6	L3N_18	24.027
74	W3	L5P_18	26.238
76	Y3	L5N_18	26.119
78	W5	L7P_18	25.073
80	W6	L7N_18	25.143
82	AA4	L9P_CC_18	30.165
84	AA5	L9N_CC_18	29.876
86	AB4	L11P_CC_18	27.630
88	AA3	L11N_CC_18	27.562
90	AD4	L13P_18	30.496
92	AD3	L13N_18	30.504
94	AC6	L15P_18	31.290
96	AB7	L15N_18	31.355
98	AD6	L17P_18	36.735
100	AD5	L17N_18	36.737

JP3 Pin	Connection	FPGA LVDS	Length (mm)
102	AE6	L19P_18	40.548
104	AE5	L19N_18	40.708
106	-		
108	-		
110	-		
112	-		
114	USB_SDA		
116	+VDC		
118	+VDC		
120	+VDC		